Development of an Electrostatically Bonded Fiber Optic Connection Technique

MARK B. SPITZER, MEMBER, IEEE, PETER R. YOUNGER, FREDERICK C. ALLARD, AND LESTER D. OLIN

Abstract—**This paper describes the development and fabrication of prototype multichannel fiber optic connector subassemblies. The design is based on state-of-the-art fabrication techniques which use anisotropic silicon etching and electrostatic bonding. The advantages of these techniques, as well as the manner in which they are employed in a fabrication sequence, are discussed in detail. It is shown that accurate fiber positioning in a two-dimensional array can be achieved without stringent control of fiber diameter. Results of fabrication of prototypes are presented.**

I. INTRODUCTION

WIDESPREAD utilization of fiber optics for signal transmission requires the development of a simple means to connect and disconnect multifiber cables. Such interconnections require high precision parts which can make them somewhat more complicated than their electrical counterparts. This paper describes a fiber optic connector technology which permits the interconnection of large numbers of fibers, with high accuracy and with excellent packing density.

The principal requirement of any multichannel fiber optic connector is high precision alignment of all fibers. This requirement severely constrains the schemes which can be applied to this end. For example, coaxial interconnect systems which connect single fibers by means of precision ferrules cannot be practically modified to handle several fibers. The coaxial concept is basically a single channel design, whereas the connector concept presented herein is basically a multichannel design capable of accurately mating many channels in a single mechanism. This concept has a further unique advantage in providing an inherent mechanism for self-centering fibers.

This concept is based on precisely etched V-groove silicon (Si) wafers which are used in pairs to locate the fibers within complementary V-grooves. Electrostatic bonding (ESB) is used for formation of a permanent bond between wafers. This design is not limited to one complementary pair; a "stack" of complementary pairs can be used to form a two-dimensional array. Unlike adhesives, the ESB process minimizes the introduction of cumulative positioning error arising from thickness variations at the Si-to-Si bond interface. As will be discussed in detail in a later section, the process also provides fiber centering within the cavity formed by the complementary V-groove pair. This centering is insensitive to small variations of fiber diameter. Thus, both a reduction in transmission loss and an economic benefit (through relaxed fiber diameter tolerance) can be attained.

A photograph of a prototype 24 channel connector subassembly is shown in Fig. 1. The subassembly consists of a V-groove Si block which contains a 3×8 array of fibers. The V-groove block is cemented to a Lucite trough which is filled with epoxy to form a strain relief to protect the unjacketed fibers. Jacketed fibers extend from the back of the subassembly.

Fig. 2(a) shows a view of the front of the V-groove block. Although it is not evident in the photograph, the monolithic V-groove block actually comprises four V-grooved silicon wafers with eight fiber grooves at each wafer interface, as shown in Fig. 2(b). The design technology employed for such a multilayer array will be discussed in Section II. Fabrication is reviewed in Section III.

II. V-GROOVE BLOCK DESIGN

Each fiber in this multichannel connector concept must be internally oriented in an array; the array is externally aligned to a mate when interconnection of two connector halves is made. In the design reported here, the accuracy of internal orientation of fibers is improved by utilizing intersecting crystal planes which form V-grooves. Reliance on the crystal structure has several advantages which will become apparent later; the most important concerns the accurate reproducibility which can be achieved [1].

The selection of silicon is based on the ease with which V-grooves are formed in it by anisotropic etching. This technology has received considerable attention in the literature [2]-[4] and will be discussed only briefly here. Anisotropic etching results from the selective etch rates of various crystal planes. There are several etches which remove Si more slowly from (111) planes than (100) or (110) planes. For example, a solution of potassium hydroxide and water, used in this work, etches (110) planes at ~1 μm/min, whereas the etch rate of (111) planes is ~2 nm/min.

The masking of silicon is straightforward using SiO_2; however, the alignment with the proper crystal axis is critical for good V-groove formation. In the connector fabrication discussed in the next section, (110) silicon wafers were used with

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M. B. Spitzer is with Spire Corporation, Bedford, MA 01730.

P. R. Younger was with Spire Corporation, Bedford, MA, 01730. He is now with the Nova Implantation Systems Division, Eaton Corporation.

F. C. Allard and L. D. Olin are with the New London Laboratory, Naval Underwater Systems Center, New London, CT 06320.

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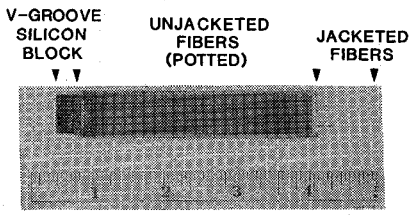
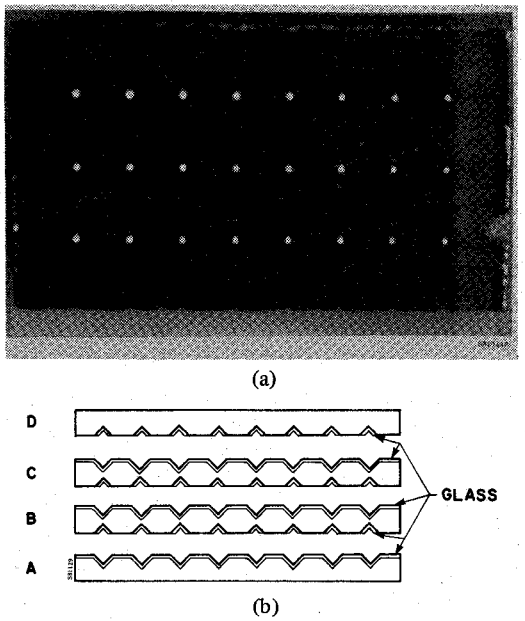


Fig. 1. Photograph of the Prototype 24 channel fiber optic connector subassembly.



(a)

(b)

Fig. 2. (a) Photograph of the front view of the 24 channel *V*-groove block. (b) Diagram of the 24 channel *V*-groove block illustrating wafer configuration.

surface orientation within 0.5° of the actual (110) planes. In addition to surface plane orientation, the mask must pattern windows with orientation parallel to the trace of the (111) plane in the (110) surface. Fig. 3 is an SEM micrograph of *V*-grooves formed in this way. The etch essentially stops when the *V*-groove is complete, making the process relatively insensitive to time, temperature, or concentration variations. The *V*-groove angle is determined entirely by the silicon crystal planes and, accordingly, does not vary. This insensitivity to process variations yields excellent process reproducibility. The accuracy of *V*-groove positioning within a single plane is limited primarily by the precision of the mask formation. In this work, such error was on the order of 1 μm. This is adequate for multimode fibers with cladding diameters of 125-140 μm; high resolution techniques can reduce this error if it is necessary when coupling core-centered single mode fibers.

Fig. 4 is an SEM micrograph of a 2 X 6 array which illustrates the complementary *V*-groove configuration. Electrostatic bonding (ESB) was used to permanently fix the silicon wafers in complementary positions [5]-[7]. In the ESB technique, a thin layer of glass is used to assist the formation of a wafer-to-wafer bond. A bond is formed between glass and silicon when an external electric field moves the positively charged alkali ions in the glass away from the interface, thus leaving negative oxygen ions, which bond to the silicon

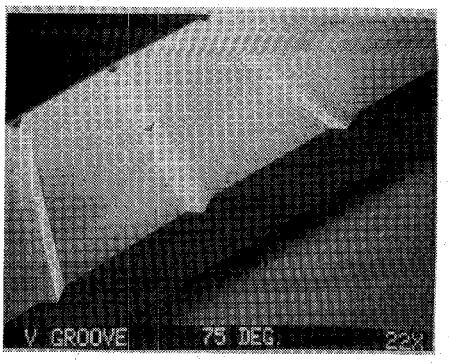
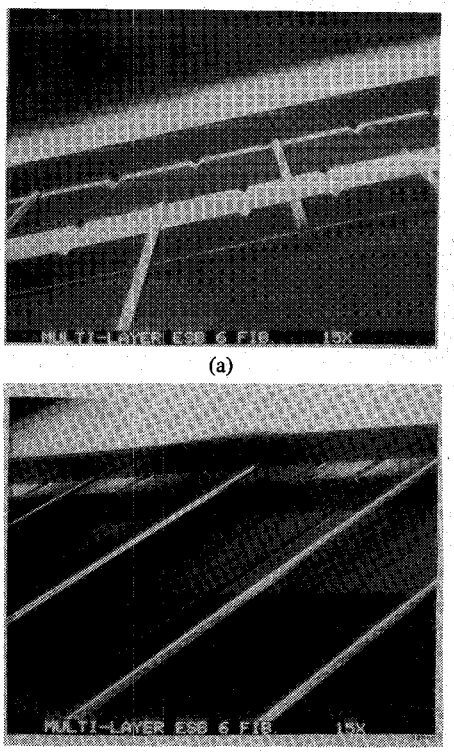


Fig. 3. SEM micrograph of *V*-grooves formed in a silicon wafer.



(a)

(b)

Fig. 4. SEM micrograph of a 2 X 6 channel configuration illustrating complementary *V*-groove structure.

across the interface. Temperatures of about 400°C are required for alkali mobility and rapid processing, but temperatures of 500-600°C are used in order to soften the glass.

The ESB type coupler requires a glass layer of at least 4 μm in thickness to permit silicon wafers to be bonded together. This layer is deposited on the wafers by a technique such as sputtering to insure very uniform thickness. This layer, simultaneously deposited in the grooves, serves as a deformable medium that can accommodate fiber diameter variations. The thickness of the glass layer must equal or exceed the diameter tolerance of the fiber. Since thick layers are uneconomical to deposit and may become stressed, it is desirable to keep the glass layer close to the 4 μm required for bonding. This thickness is consistent with anticipated fiber products.

This hard glass layer which accommodates fiber variation also allows for automatic fiber centering. The glass layer will support the symmetric deformation forces provided by the

complementary V-groove assembly. The fiber remains centered in the channel at the plane of the wafer-to-wafer interface, owing to the symmetric forces which are largely independent of fiber diameter.

The accuracy with which glass layers can be deposited is a major advantage of ESB. For the 24 fiber elements shown in Fig. 1, three glass layers are required. If independent (i.e., nonmatched) connectors are to be made, accumulated wafer and bond layer thickness tolerances must be kept to a minimum. This is not easily accomplished with adhesives, but sputter deposition is well suited to glass layer thickness control (as well as uniformity).

A potential problem in the electrostatically bonded device is the internal stresses caused by the differential thermal expansion of the silica fiber and the silicon. The two are locked together when the deformable glass layer between them hardens, at a temperature between 500 and 600°C. As the device cools to room temperature, the greater contraction of the silicon places the wafer in radial compression and longitudinal tension. The fiber is correspondingly in radial and longitudinal compression, but its strength is many orders of magnitude greater than the stresses to which it is subject.

A straightforward, finite element analysis indicates that the radial compression in the silicon at the point of contact with the fiber, on cooling to room temperature, is on the order of 7 kpsi. This is lower by an order of magnitude than the breaking strength of silicon in compression. Although the force on each wall of the groove is compressive, the silicon is in tension at the vertices of the groove. For the Rhombic cross section chosen, there is a tensile stress of about 4 kpsi at the obtuse vertex, in the silicon, and one of 6 kpsi across the bonded interface. The stress in the silicon is still well below its fracture strength in tension (30 kpsi). There are no data available on the tensile strength of the silicon-silicon bond, but experience with other glass-silicon bonds indicates that it should be at least as strong as the silicon itself.

A similar calculation of the longitudinal stress in the silicon indicates a stress of approximately 24 kpsi. This value is near the fracture strength of the silicon; however, no stress-related problems have been detected to date.

III. Connector Subassembly Fabrication

The material from which the fiber alignment components were made was p-type silicon in wafer form. The surfaces were polished and flat to within ±1 μm across the wafer surface [8]. The orientation of the surface was within 0.5° of the (110) plane.

Fig. 5 illustrates the crystal geometry and V-groove angles attainable on (110) and (100) wafers. The (110) orientation was chosen for this work because the wider groove angle results in shallower V-grooves.

A thermal oxide (0.7 μm) was grown on the wafers in a wet atmosphere and an etch mask was prepared using standard photolithographic techniques. Positioning error of the image in the photomask preparation was limited to 1 μm. Fig. 6(a) illustrates the wafer configuration after HF etching of the oxide.

As discussed in the previous section, a potassium hydroxide

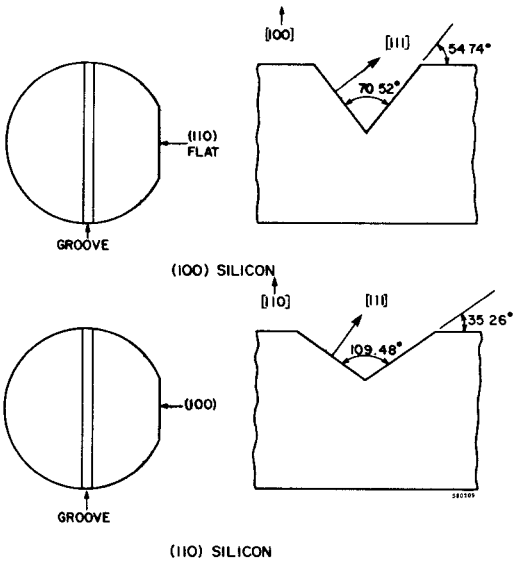


Fig. 5. V-groove geometry for two silicon orientations.

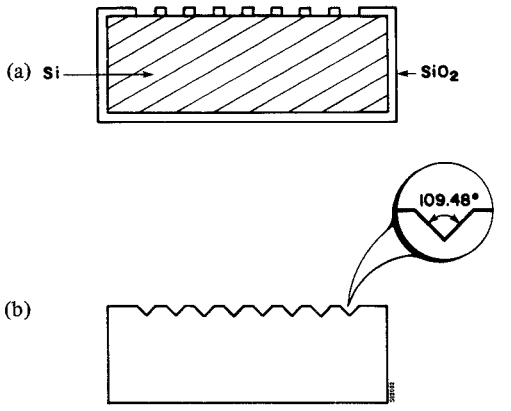


Fig. 6. Eight channel V-groove configuration. (a) Wafer configuration after HF etch. (b) Wafer after preferential etch and removal of oxide mask.

(KOH) and water solution was used for anisotropic etching [3]. The etch rate in the (110) direction is more than two orders of magnitude greater than either the rate in the (111) direction or the SiO_2 etch rate. Thus, groove positioning error because of oxide undercutting or (111) etching is negligible. Fig. 6(b) illustrates the wafer configuration after anisotropic etching.

To utilize the ESB process in this application, one surface (but not both) at each Si-Si interface must be glass coated. In our work on this subject it has been found that sputtered Corning 7070 glass is well-suited to this purpose. A thin glass layer was deposited on each silicon wafer. Sputter deposition resulted in glass layers typically 4-5 μm thick and uniform to within 1 μm. Since glass was deposited on all components (so as to be present in all V-grooves), it was necessary to remove the glass from one half of the bond surfaces to achieve a glass-silicon bond. The glass was therefore suitably masked and etched in HF.

The 3 × 8 array shown in Fig. 2 was fabricated by stacking four wafers with V-grooves etched in both sides. The use of ESB allows the wafers to be stacked without accumulation of

positioning error because the glass thickness is well controlled. This is an important advantage of this process. A larger array can be fabricated, but this has not been attempted.

Bonding involves the application of temperature, pressure, and electric field, but is straightforward. During the bond, the sample was heated to 580°C to soften the glass, and application of pressure forced the fibers to deform the glass layer within the grooves. Since the fiber-glass layer contact is symmetrical, the fibers center themselves within the double groove cavity.

After bond formation, the strain relief was fabricated. A Lucite trough was cemented to the bonded wafers and filled with epoxy. In this way the unjacketed fibers were "potted" and protected. The voids between the *V*-groove walls and the fibers were impregnated with low viscosity epoxy by pumping on the front of the connector, drawing the epoxy from the strain relief through the voids and out the front of the connector. A clear epoxy was used in our work so that we could inspect the post-potted fibers; the proper choice of epoxy (for mode stripping) was not identified.

The *V*-groove block shown in Fig. 2 is one of 18 connector subassemblies fabricated in this way. This experience with prototype fabrication indicates the potential for the manufacture of this design.

IV. Insertion Loss

The fibers incorporated in the connector were step-index ITT type 121, with a measured core diameter of 100 ± 5 μm, a cladding diameter of 140 ± 7 μm, and a numerical aperture of 0.3. The insertion loss for the utilization of this fiber in the *V*-groove design has been estimated by assuming the alignment error which might arise from worst case tolerance accumulation. For this estimate, the equations presented by Thiel and Hawk [9] have been used to calculate the loss encountered with step-index fiber, assuming uniform distribution of energy over all modes.

The core diameter variation results in significant insertion loss. Maximum mismatch in core diameter yields attenuation of 0.43 dB. At the actual surfaces of the connectors that were fabricated, it was found that the core did indeed vary over the stated tolerance range.

The effect of lateral displacement has also been estimated. The variation in flatness of each silicon piece was limited to ±1 μm. Thus, for an eight channel (single layer) connector, the displacement is limited to 2 μm. Since the cladding diameter tolerance was 7 μm, the total displacement, in the absence of fiber centering, could be as large as 9 μm. For 95 μm core, the insertion loss is 0.56 dB. With fiber centering, the displacement is reduced to 2 μm, thus reducing the loss to 0.12 dB.

Displacement in a 24 channel connector can arise from variation in the glass layer thickness, which is controlled to approximately 1 μm. For three glass layers, the displacement can be as large as 5 μm, assuming fiber centering, which yields an insertion loss of 0.16 dB.

The connection surfaces were polished to a flatness of ±0.5 μm. The silicon was first oriented by X-ray crystallographic techniques so that the resulting polished surface was within 0.5° of the equivalent (110) plane. In this way, end separation was limited to 1 μm (0.06 dB) and angular misalignment to 1° (0.17 dB).

TABLE I
Attenuation Measurement for Each Channel in the Eight-Fiber Connector

Channel Number	Attenuation (dB)	
	Dry	Index Matching Gel
1	1.47	1.06
2	1.14	0.81
3	1.29	0.89
4	1.63	1.11
5	1.30	0.96
6	1.37	1.07
7	1.60	1.42
8	1.59	1.37
Average	1.42	1.09

The upper limit to the total insertion loss in the eight channel connector is the sum of the worst-case losses and is 0.78 dB, if perfect fiber centering is achieved, and 1.22 dB without fiber centering. Fresnel reflection losses can add another 0.4 dB to the insertion loss, making the upper limit 1.62 dB.

Attenuation measurements were recently obtained for a butt-coupled eight fiber subassembly. Using a throughput-loss measurement technique incorporating a controlled input to the *V*-groove pigtails, an average loss of 1.42 dB was obtained with a dry interface. With an index matching gel, the average loss was 1.09 dB. The data for all eight fibers are replicated in Table I.

These measurements are in agreement with the above estimates of insertion loss. At the present time, we attribute the variation in loss to displacement arising from variations in the amount of fiber centering achieved. Such variation would occur if the glass layer within the *V*-grooves were less than 4 μm; a thinner glass layer would make the connector more sensitive to fiber diameter variations. Improved fibers with tighter cladding diameter tolerance have recently become available; use of such fibers with the *V*-groove connection technique would offer a greater reduction of displacement loss.

V. Summary

This paper has presented a review of the ongoing development of a multifiber optic connector subassembly. The technology uses silicon *V*-groove etching and electrostatic bonding to achieve state-of-the-art precision in fiber positioning. Since both vertical and horizontal fiber positioning are possible, allowing high fiber packing density, the design is particularly applicable to fiber optic cable interconnects.

The work reported here has focused on the design and fabrication of the fiber alignment element. To date, 18 prototype connector subassemblies have been fabricated in this way. Work currently in progress is aimed at development of a simple interconnection for macroalignment of the connector subassemblies. In addition, further evaluation of the optical aspects of this design is underway.

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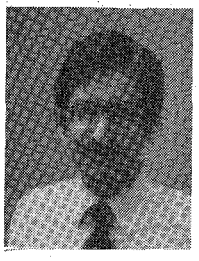
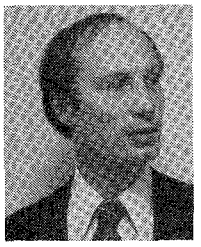


Mark B. Spitzer (S'78–M'81) received the B.A. degree in physics from Boston University, Boston, MA, in 1975 and the M.Sc. and Ph.D. degrees in physics from Brown University, Providence, RI, in 1977 and 1981, respectively. His thesis work concerned the theoretical upper limit to the conversion efficiency of photovoltaic devices.

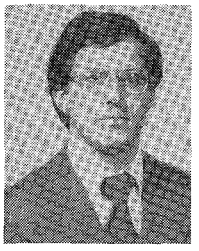
While at Brown University, he was designated as the Amperex Electronic Corporation Fellow in Applied Research. In 1980 he joined the technical staff of Spire Corporation, Bedford, MA, where his work is primarily concerned with the use of silicon for device fabrication. In addition to this work with fiber optic connectors, he is responsible for the development of ion implantation processing of low-cost sheet silicon.

Dr. Spitzer is a member of the American Physical Society and the Materials Research Society.



Peter R. Younger received the A.B. degree in physics from Cornell University, Ithaca, NY, in 1966 and the A.M. and Ph.D. degrees in physics from Boston University, Boston, MA, in 1968 and 1975, respectively. His research at Boston University involved measurement of the thermophysical properties of cesium at high temperature and pressure.

In 1976 he joined Spire Corporation, Bedford, MA, where his work concerned electrostatic bonding process development. More recently, he has been involved in the development and production of high-efficiency solar cell arrays. In 1982 he joined the Nova Implantation Systems Division, Eaton Corporation, where his work is involved with ionized cluster beam technology for film deposition.



Frederick C. Allard was born in Lowell, MA, on August 4, 1943. He received the B.S. degree in physics from Providence College, Providence, RI, in 1965 and the M.S. degree in optical sciences from the University of Arizona, Tucson, in 1969.

Since 1965 he has been with the Naval Underwater Systems Center, New London, CT, where he is currently Fiber Optics Manager. His activities have included optical system analysis, the development of test instrumentation for submarine periscopes, and the application of fiber optics and related electrooptic technologies to submarines. He is a member of several Department of Defense working groups whose functions range from technology assessment and technology exchange to technology export control.

Mr. Allard is a member of the Optical Society of America.

Lester D. Olin was born in New York, NY, on April 30, 1943. He received the B.S. degree from the Rochester Institute of Technology, Rochester, NY, in 1965 and the M.F.A. degree from Ohio University, Athens, in 1968.

Between 1968 and 1970 he was a Photographic Systems Engineer at Data Corporation, Dayton, OH (now Mead Technology Laboratory), where he was assigned to technical support of the Air Force's Southeast Asia aerial reconnaissance operations and the NASA Apollo program. In 1973 he joined the staff of the Naval Underwater Systems Center, New London, CT, one of the principal research and development laboratories supporting the Navy's submarine fleet. He has performed research and related photooptical systems and is currently working in the area of optomechanical design of through-hull fiber optic systems.

Mr. Olin is a member of the Society of Photo-Optical Instrumentation Engineers.